IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended): A distributed data cache coupled to one of a plurality of ~~heterogeneous processing~~ reconfigurable execution nodes (RXN), wherein the heterogeneous processing nodes are coupled by a programmable interconnection network having a network root and a plurality of crosspoint switches, the distributed data cache comprising:

a ~~first~~ plurality of cache memory ~~unit~~ units each having a plurality of cache ports; ~~and~~

a plurality of data buses connected with each of the cache memory ~~unit~~ units, wherein each of the plurality of data buses is connected with one of the plurality of cache ports of the cache memory ~~unit~~ units; and

the reconfigurable execution node adapted for processing data and having at least one data input and at least one data output, wherein the data input and data output are connected with the plurality of data buses.

2. (Cancelled)

3. (Currently Amended): The distributed data cache of Claim ~~2~~ [[1]], further comprising a multiplexer for alternately connecting the data input with each of the plurality of data buses.

4. (Currently Amended): The distributed data cache of Claim ~~2~~ [[1]], further comprising a multiplexer for alternately connecting the data ouput with each of the plurality of data buses.

5. (Previously Presented): The distributed data cache of Claim 1, further comprising a plurality of data address generators connected with a memory unit and the plurality of data buses.

6. (Previously Presented): The distributed data cache of Claim 5, wherein the plurality of data address generators are adapted to retrieve a plurality of data values from the memory unit and communicate the plurality of data values to the plurality of data buses.

7. (Original): The distributed data cache of Claim 6, wherein the plurality of data address generators are adapted to simultaneously communicate the plurality of data values to the plurality of data buses, wherein each of the plurality of data value is communicated to a different one of the plurality of data buses.

8. (Original): The distributed data cache of Claim 7, wherein the first cache memory unit is adapted to simultaneously load a plurality of data values from the plurality of data buses, such that each of the plurality of data values is loaded in a different one of the plurality of cache lines of the first cache memory unit through the same port.

9. (Original): The distributed data cache of Claim 1, wherein the number of cache lines of the first cache memory unit are equal to the number of data buses.

10. (Original): The distributed data cache of Claim 1, further comprising at least one additional cache memory unit also having a plurality of cache lines, wherein each cache line of the additional cache memory unit is connected with the plurality of data buses.

11. (Original): The distributed data cache of Claim 10, wherein the total number of cache memory units is equal to the number of cache lines in each cache memory unit.

12. (Currently Amended): An apparatus for transferring a plurality of data values arranged in a matrix, the apparatus coupled to one of a plurality of heterogeneous processing nodes, wherein the heterogeneous processing nodes are coupled by a programmable interconnection network having a network root and a plurality of crosspoint switches, the apparatus comprising:

a plurality of cache memory ~~unit~~ units, each cache memory unit having a plurality of cache ports; and

a plurality of data buses, each data bus connected with a different one of the plurality of cache ports from each of the cache memory or register file units.

13. (Currently Amended): The apparatus of Claim 12, further comprising a plurality of data address generators adapted to retrieve a plurality of data values from the memory unit and communicate the plurality of data values to the plurality of data buses, the apparatus being configured to transpose a matrix stored in the main memory by reading a matrix comprising a plurality of row elements from the main memory into the plurality of data buses, then simultaneously transferring the row elements to the cache ports of one of the cache memories, and repeating the operation for each row of the stored matrix.

14. (Original): The apparatus of Claim 13, wherein the plurality of data values comprises a plurality of sets of data values.

15. (Previously Presented): The apparatus of Claim 14, wherein the plurality of data address generators are adapted to sequentially communicate the plurality of sets of data values with the plurality of data buses.

16 – 18 (Cancelled)

19. (Original): The apparatus of Claim 16, wherein each of the cache memory units is adapted to simultaneously load one of the sets of data values from the plurality of data buses, such that each data value of the set of data value is loaded in a different one of the plurality of cache ports of the cache memory unit or register file.

20. (Currently Amended): A method for transferring a plurality of data values arranged in a matrix to transpose the matrix, the matrix including a plurality of heterogeneous processing nodes coupled by a programmable interconnection network having a network root and a plurality of crosspoint switches, the method comprising:

retrieving a first subset of data values from the plurality of data values from a memory unit storing the matrix in rows;

simultaneously transferring the first subset of data values comprising one of the rows of the matrix; to a plurality of data buses, wherein each data value of the first subset is transferred to a different one of the plurality of data buses; ~~and~~

simultaneously loading the first subset of data values from the plurality of data buses to a first cache memory unit having a plurality of cache ports, wherein each cache port receives a data value from a different one of the plurality of data buses to define a column of the matrix; and

repeating the operation for each row of the matrix to complete transposing of the matrix.

21. (New): The distributed data cache of claim 1, wherein the RXN includes a plurality of selectively configurable elements each having a configuration determined by the value of a multi-bit control word, the bits being simultaneously supplied in one or more of the control words stored in the cache memory units over the data buses.

22. (New): The distributed data cache of claim 21, wherein the RXN is adapted to be reconfigured to perform a sequence of operations responsive to a sequence of the control words.

23. (New): The distributed data cache of claim 22, wherein each of the memory units comprises a plurality of cache lines, each cache line being associated with one of the plurality of cache ports, each cache line storing one of the control words, the sequence of control words being retrieved by an index uniquely identifying the cache line, a sequence of the indexes defining a single access control word.

24. (New): The distributed data cache of claim 23, wherein the access control world is identified by a flag bit, the remainder of the access control word comprising a sequence of indexes.